lar, the author also wishes to thank E. J. Guertin of AT&T Long Lines.

REFERENCES

[1] G. L. Matthaei and E. G. Cristal, "Theory and design of diplexers and multiplexers," in *Advances in Microwaves*, vol. 2, L. Young, Ed. New York: Academic, 1967, pp. 237–326.
[2] N. Marchard, "Transmission line conversion transformers," *Electronics*, pp. 142–145, Dec. 1944.
[3] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*. New York: McGraw-Hill, 1964, pp. 440–450 and 595–605.
[4] C. E. Fay and R. L. Comstock, "Operation of the ferrite junction circulator," *IEEE Trans. Microwave Theory Tech.* (*1964 Symposium Issue*), vol. MTT-13, pp. 15–27, Jan. 1965.
[5] D. Masse, "Broadband microstrip junction circulators," *Proc. IEEE* (Lett.), vol. 56, pp. 352–353, Mar. 1968.
[6] D. C. Hanson and W. W. Heinz, "Integrated electrically tuned X-band power amplifier utilizing Gunn and IMPATT diodes," *IEEE J. Solid-State Circuits* (*Special Issue on Microwave Integrated Circuits*), vol. SC-8, pp. 3–14, Feb. 1973.
[7] C. Y. Pon, "Hybrid-ring directional coupler for arbitrary power divisions," *IRE Trans. Microwave Theory Tech.*, vol. MTT-9, pp. 529–535, Nov. 1961.
[8] *Transmission Systems for Communications*, Western Electric Co., Winston-Salem, N. C., Tech. Publ., 1971.

Reliability Testing of Microwave Transistors for Array-Radar Applications

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***Abstract*—Solid-state array radar is of great current interest because of the inherent reliability of solid-state devices and the concomitant promise for improvement in system reliability. However, no extensive reliability base has been established for solid-state devices employed under radar operating requirements. In this paper some of the important factors bearing a device reliability are treated. Accelerated life tests under RF conditions are presented for L-band power transistors. Preliminary life-test and failure-analysis data are also presented with recommendations on how the information can be used by the radar systems designer.**

I. INTRODUCTION

SEMICONDUCTOR devices are inherently more reliable than vacuum tubes because no materials are consumed during operation and high g applications can be satisfied. The diffusion profiles are stable for hundreds of years even at severe operating conditions; however, reactions between metal contacts and Si or SiO_2, manufacturing defects, oxide-stability problems, lack of adequate designed-in ruggedness, and other similar factors can limit the reliability of these devices. Failure rates of 0.001 percent/1000 h have been established for some devices. The success of the Minuteman missile program is an excellent example of solid-state reliability.

Solid-state radar requirements, however, impose unique stresses for devices. The devices must be qualified for these special operating stresses in order to establish confidence that premature system failure will not occur.

Bipolar microwave power transistors, similar to that shown in Fig. 1, are often employed in the class C amplifiers that comprise transmitter subsystems. These transistors are multicell devices which are subjected to severe stress (depending on power-level requirements) during pulsed-radar operation. For this reason, it is believed that these particular components are the critical elements in achieving long system life. This paper will outline efforts to establish reliability of L-band power transistors for phased-array radar applications.

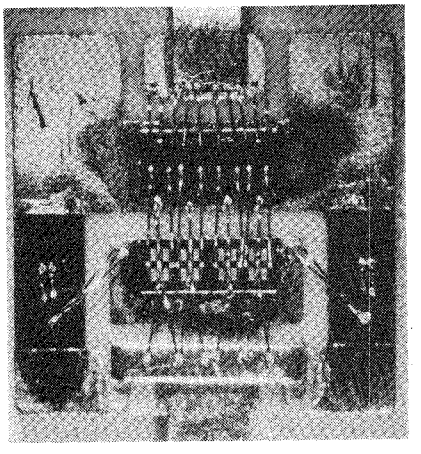

Fig. 1. Typical L-band bipolar microwave transistor.

II. FACTORS AFFECTING RELIABILITY

There are three major classes of failures for any system. These are illustrated in Fig. 2 and consist of: 1) infant mortality—failures which can often be traced to defects; 2) random failures; and 3) wearout failures which inclued

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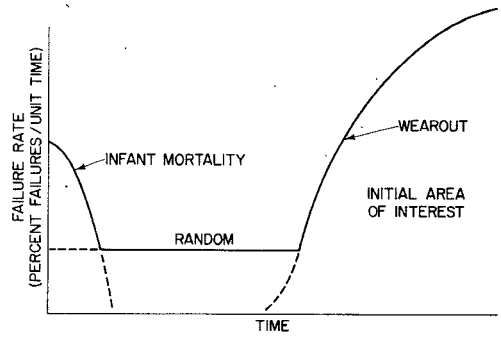


Fig. 2. Major classes of failures.

TABLE I
FACTORS AFFECTING TRANSISTOR RELIABILITY

I. Basic Device Design
- A. Cell Design
  - Configuration
  - Ballasting
  - Size/Number of Cells
- B. Metalization
  - Current Density
  - Barrier Integrity
  - Metal Reactions
- C. Internal Matching
  - Load Balancing
- D. Efficiency

II. Temperature
- A. (Thermal Impedance Efficiency)
- B. Pulse Related Temperature Excursions
- C. Heat Sinking
- D. Thermal Stability
  - Resistance to Second Breakdown
  - Hot Spots

III. Quality Assurance
- A. Process Controls
- B. Effective Screens
- C. Traceability

IV. Externally Induced Stresses [Ref. 1]
- A. Circuit Interface
- B. System Environment
- C. Heat Sinks

reactions which degrade the devices. The first major step in attaining reliability is to assure that no inherent wearout mechanisms will fail devices and cause premature failures during the required system life. Additional work on process-control and screening procedures can then be instituted to improve overall reliability.

When failure mechanisms have been identified and evaluated for a given level of stress, the following two alternatives are available to the system engineer.

1) If the wearout mechanisms are not a significant factor for the required system life, a circuit can be designed to limit the externally imposed stresses on the device to acceptable levels.

2) Devices can be redesigned to obviate or minimize the wearout mechanisms and the device can then be qualified by additional stress testing.

A tradeoff analysis is necessary based on cost, probability of device improvements, increase in system complexity, and/or reduction of system performance.

There are at least four interdependent factors which affect transistor reliability and thus system reliability. This is true for all the three classes of failure previously mentioned. These are outlined in Table I.

III. TESTING CONCEPTS FOR IDENTIFYING WEAROUT MECHANISMS

Three categories of accelerated life tests are outlined in Table II. Despite the additional complexity and cost, pulsed RF life testing is considered to be a key approach of accelerated life testing. This technique most closely simulates actual conditions and does not exclude effects that cause failures at lower stress levels under RF conditions. All of the testing described herein is performed under pulsed RF conditions. However, additional dc tests and oven-type tests should be made concurrently to accelerate independent failures.

Semiconductor failure mechanisms are usually characterized by an exponential temperature dependence described by (1).

$$R = A \exp(\phi/kT) \tag{1}$$

where

- R rate of reaction;
- ϕ activation energy (eV);
- k Boltzman's constant (8.617×10^{-5} eV/K);
- T temperature in degrees Kelvin;
- A constant related to device configuration.

When reaction rate is plotted (on semilog paper) as a function of $1/T$, the result is a straight line as indicated in Fig. 3. This is the well-known Arrhenius relationship often employed in obtaining projections of semiconductor-device life. The time to failure of a particular device is the product of rate and time, a median time to failure (MTF) projection can be made by connecting data points resulting from a series of tests at different stress temperatures. Each data point represents the time at which 50 percent of a group of devices under test at a particular temperature level failed. For the purpose of transistor testing under pulsed conditions, "temperature" is defined as the peak device junction temperature; it is usually held fixed during

TABLE II
TYPES OF LIFE TESTS

TEST	ADVANTAGES	DISADVANTAGES
1. Oven	Inexpensive	Very poor correlation with rf test data
2. DC Fixed	Simple test fixtures Inexpensive	Poor correlation with rf test data due to: Device Q Power distribution Realistic stresses
Pulsed	Higher stress levels possible Simulates pulsed operation relatively inexpensive	Poor correlation with rf test data
3. RF		
CW	More nearly simulates Actual system operating conditions	More complex testing facilities Excludes thermal excursion effects
Pulsed	Simulates system operating conditions	Very complex rf testing facilities required. Necessary to raise background temperature at low duty factors to achieve high peak junction temperatures for short period tests. External circuitry limits testing above 350°C.

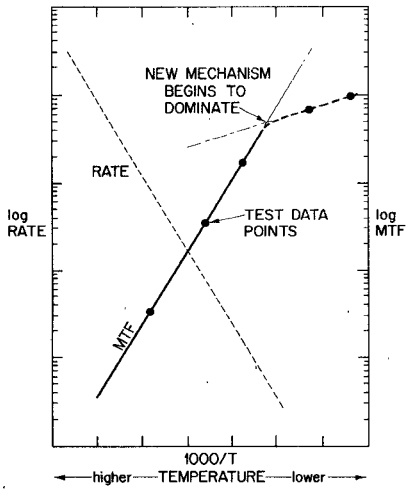


Fig. 3. Median time to failure and failure rate versus temperature.

the test. If the MTF is a straight line through a series of data points, the presence of a single, thermally activated failure mechanism is indicated for the transistors under test.

Commonality among wearout mechanisms can be anticipated even though the existence of identical failure distributions is unlikely. Variations in device configurations, in processes (which are usually considered proprietary), and in metallization schemes are expected to result in significant differences between manufacturers. Within the same device family, however, similar results are expected.

A single failure mechanism will usually dominate over a wide range of test temperatures. The advantage of accelerated testing is that inherent device-failure mechanisms can be observed in reduced periods of time at elevated temperature stress levels. While the Arrhenius relationship can be used very effectively for accelerating major failure modes and predicting life, it must be used with care. It is inappropriate to extrapolate over several orders of magnitude in time because a failure mode with a lower activation energy can dominate at lower temperatures (and long times), as illustrated by the break in the MTF curve shown in Fig. 3. In an extreme case, the failure mechanism is not accelerated and might even be decelerated at higher temperatures. An example of a failure mechanism which to first order is not accelerated by high temperatures is the restructuring of Al metal films illustrated in Fig. 4 [2]. In this example, an Al film was subjected to a thermal excursion of 57°C for 22 000 cycles. A similar test at a higher base temperature but using the same 57°C excursion resulted in the same degree of restructuring. The restructuring effect is significantly reduced in production devices by SiO_2 overcoating of the Al fingers.

In order to enhance confidence in life projections, it is necessary to conduct meaningful transistor-reliability investigations at three or more elevated peak junction temperature stress levels. The absolute levels of these various temperatures should be separated as far as possible commensurate with allowable testing schedules. Furthermore, the lowest stress level must be chosen to fail the devices in the longest practical time period. This will reduce the inaccuracies inherent in extrapolating over several orders of magnitude to normal operating conditions.

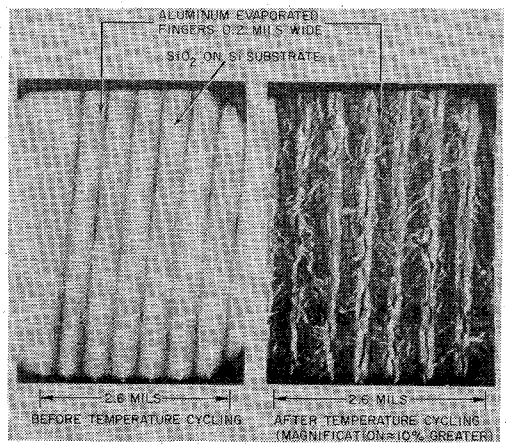


Fig. 4. Effects of rapid thermal cycling on aluminum metallized finger patterns.

TABLE III
NRL-SUPPORTED TRANSISTOR RELIABILITY EFFORTS

EFFORTS	CONTRACT NUMBER	CONTRACTOR	DEVICE
(1)	N00014-72-C-0472	Microwave Semiconductor, Inc., Somerset, N. J.	MSC-1330A (Al) MSC-1330B (Al) Long & Short Pulse Conditions
(2)	N00014-73-C-0121	RCA Semiconductor Div., Somerville, N. J.	TA-8694 (Al) TA-8777 (Au)
(3)	N00014-73-C-0214	Westinghouse Baltimore, Md.	PHI-1520A (Au)

IV. PROGRAMS AND PROBLEMS IN EVALUATING VARIOUS TRANSISTORS

In order to estimate failure rates in a finite period of time, accelerated life tests have been conducted by industry and supported by several cooperating government agencies from the various services. The Naval Research Laboratory is presently sponsoring the programs tabulated in Table III.

All testing has been performed under pulsed RF conditions in single-stage amplifier test fixtures similar to the one shown in Fig. 5. No life-test data are available from the RCA and Westinghouse tests. Microwave Semiconductor Corporation (MSC) test data on the MSC and 1330A and MSC 1330B are presented in Section V.

Several techniques are being used for maintaining a constant peak junction temperature throughout the duration of the tests. One method makes use of a common hot plate for all devices under test to set the background temperature at a suitable fixed level. This temperature, when added to the thermal excursions of the individual pulsed RF devices brings peak junction temperatures to the desired stress levels, as shown in Fig. 6. These stress

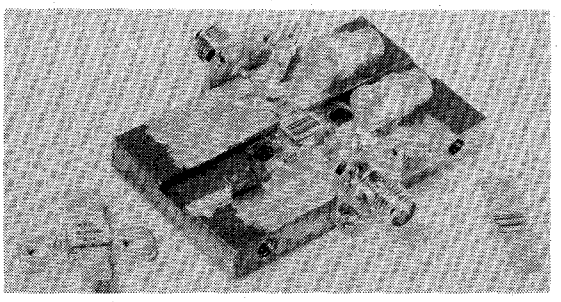


Fig. 5. Transistor test fixture.

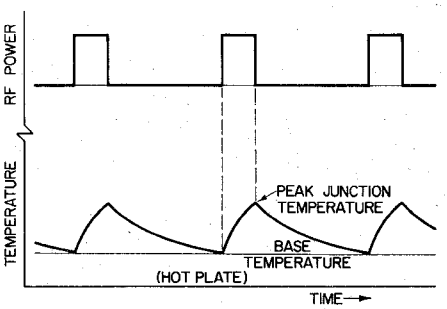


Fig. 6. RF power output and peak junction temperature versus time.

levels will result in failures in a short period of time. The dissipation in the devices is adjusted by changing tuning to bring all devices to the same temperature. As the devices degrade, the dissipation is further adjusted by detuning. Problems with this approach are associated with movement of the hot spot as a function of the complex impedance seen by the devices and the ability of the devices to withstand mismatch.

The alternative to this approach is an individually controlled hot plate for each device circuit unit. The hot plates can be adjusted to bring all peak junction temperatures to the desired stress level and can be adjusted during the test to maintain the peak junction temperature. This approach eliminates problems associated with detuning, but is more complex. If detuning is not used to increase dissipated power, a higher base temperature must be maintained for the same peak junction temperature. The higher base temperature may have deleterious effects on the circuits.

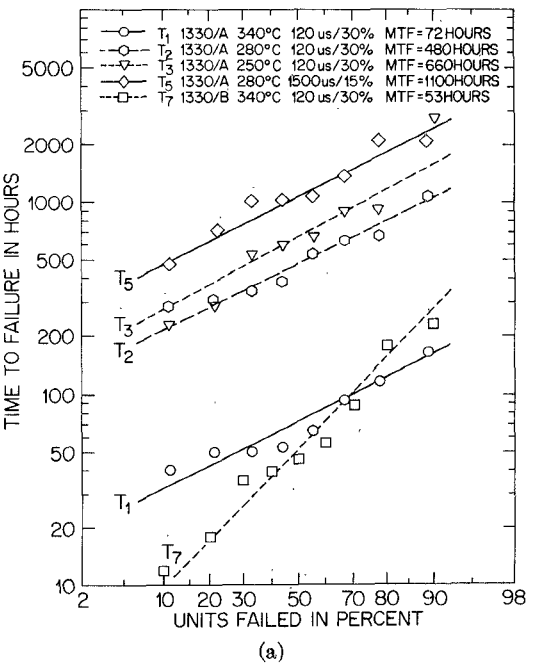
Hermeticity of packages versus continuous monitoring of temperature is another major tradeoff. Nonhermetic packages can cause potential problems from moisture or contaminants. However, the most accurate method for measuring peak junction temperature is monitoring IR emission which cannot be done on a sealed package. It is possible to keep total dissipation constant, in a sealed device package, during the test by detuning or by raising hot-plate temperature as the device degrades. However, attempts to maintain constant peak temperatures with hermetically sealed devices have introduced significant errors as the devices degraded. At this time, it appears that the better alternative is to monitor open devices using IR. The loss of hermeticity is not expected to be a serious problem since moisture accumulation is not a major factor during tests. The gold metallized devices and the SiO_2 passivated aluminum metallized devices are also less susceptible to contamination than older device types.

Regardless of the approach employed, the device output power is reduced considerably (as much as 3 dB) at very high peak junction temperatures required for initial short-period testing. This effect can tend to mask the presence of other failure mechanisms as noted in Section III.

V. STRESS-TEST DATA

Pulsed RF testing was performed on the emitter-ballasted Microwave Semiconductor Corporation MSC 1330A and MSC 1330B devices. RF pulsewidths of 1.5 ms and 120 μs were employed at 15 and 30-percent duty factors, respectively. The different pulsewidths and duty factors were selected in order to relate typical radar parameters to device life. Previously screened devices were mounted in tunable amplifier test jigs (Fig. 5) and sequentially evaluated at three different peak junction temperatures: 340°C, 280°C, and 250°C. Typically, a group of eight devices was tested at each temperature; junction temperatures were maintained by external circuit tuning. The background temperature for each group of devices was controlled by a hot plate.

Results of tests to date are shown in Fig. 7(a) for the 1330A devices and in Fig. 7(b) for 1330B devices. The B device operates over the same frequency-power range as the A device, but has tighter geometries, fewer cells, and higher efficiency. These log-normal plots Fig. 7(a) and (b) indicate the time to failure for each of the individual devices in each temperature stress group. A failure was defined as a reduction in output power of 3 dB. No catastrophic failures were observed during the tests. It is noted that failures are not located symmetrically about the point in time at which 50 percent of the devices failed. From the slopes of these log-normal plot rate-time curves, failures are attributed to a wearout mechanism and not to random



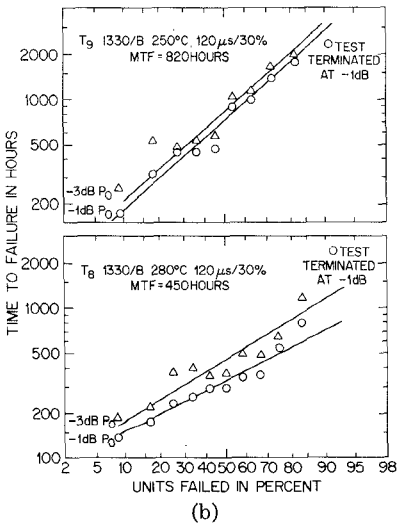


Fig. 7. Transistor test results.

statistical failures. Had the observed failures been random at the 280°C temperature level, the curve would have been shaped as indicated in Fig. 8 by the solid points. Infant-mortality failures would have placed some devices on an initial slope even steeper than the slope for random failures. Thus, in this case, the method employed by MSC was an effective device screen. Similar reason applies to other temperature levels. Median points of failure at the various peak junction temperature levels are shown on Fig. 9 and are the basis for the Arrhenius plot. This curve can be used to estimate device life at normal operating conditions; however, it is noted that the degradation in output power was not linear and is shown in Fig. 10 for a typical device.

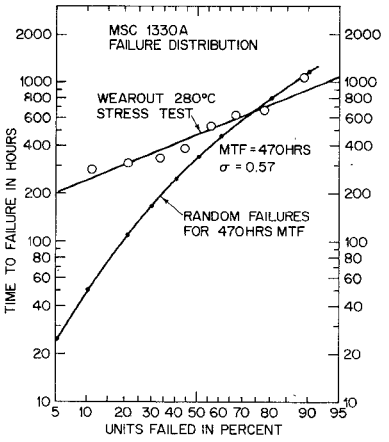


Fig. 8. Comparison of wearout to random failures at 280°C.

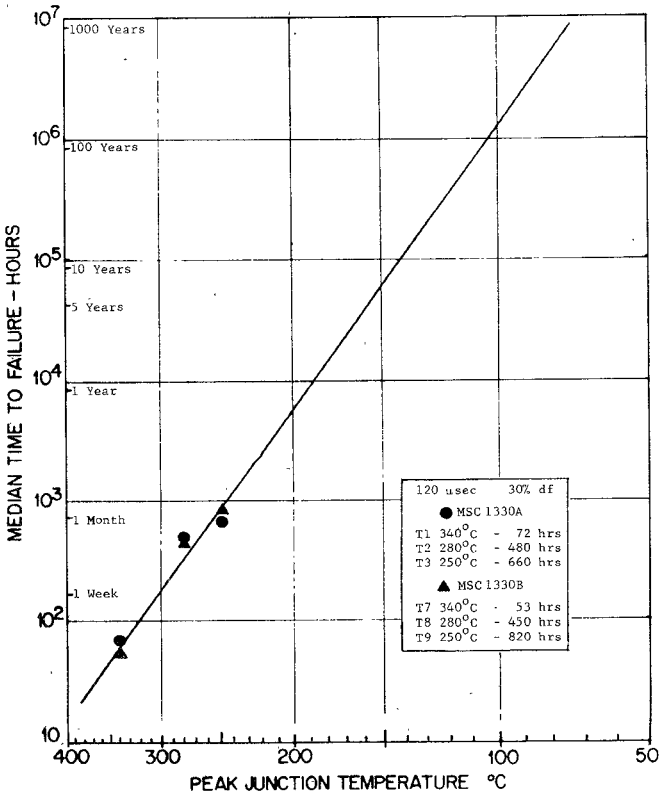


Fig. 9. Median time to failure versus stress temperature levels.

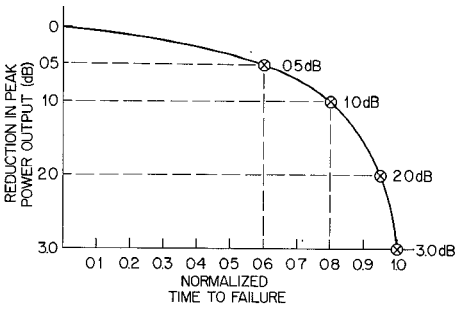


Fig. 10. Reduction in peak power output versus time.

A sample MTF calculation in Table IV indicates how to use the data from Fig. 9. The thermal impedance is typical of the MSC 1330 power transistor for the pulsewidth and duty factor used. The peak junction temperature is then calculated from thermal impedance and efficiency. The efficiency numbers of Table IV are conservative, but typically run 5–10 percent higher for the B device. In Fig. 9, the MTF for the B device did not differ significantly from the A device for the same temperature. The implication of this analysis is indicated in Table IV. The improved efficiency and same thermal resistance implies a longer MTF for the same operating conditions. The A and B devices are designed to operate at the same frequency and power levels, but the B device has closer spacings and fewer cells and operates with a higher efficiency.

Additional data not included in Fig. 9, indicate that to first order for a given peak junction temperature and pulsewidth, the MTF is inversely proportional to duty factor [3]. The 1500-μs 15-percent duty factor (DF) results included in Table IV are a portion of these data.

The tests for $T1$–$T9$ were performed on hermetically sealed transistors. An effort was made to maintain constant temperature during life test using detuning to keep power dissipation constant. This technique worked reasonably well for the 12-cell 1330A, but discrepancies of more than 20°C were noted on a few of the 8-cell 1330B devices. While the temperature error probably did not occur for the major segment of the test, this does not point out the need for continuous monitoring of temperature.

Another irregularity was observed at the 250-deg stress

TABLE IV
EXAMPLES OF MSC 1330 MTF CALCULATIONS

PARAMETER	MSC 1330A 12 Cells		MSC 1330B 8 Cells	
Pulse Width; microseconds	120	1500	120	1500
Duty Factor; %	30	15[a]	30	15[a]
Collector Efficiency; η_c in %	55	55	60	60
Power Dissipation at 30 Watts Peak Output	28.5	28.5	24	24
Thermal Impedance (θ_{jc}); °C/Watt	1.4	2.4	1.4	2.4
Temperature Rise (ΔT); °C	40	68	33	57
Peak Junction Temperature (T_{pj})	75	103	69	92
Median Time to Failure; hours (x 10^6)	6	2	10	3

Note: For a 35°C system background temperature.
[a] Refer to Section V for factor of 2 in MTF compared to 120 μs.

level. The initial group of A devices had a shorter life than expected based on predictions from the results of the two previous higher temperature tests. Examination of previous screening data revealed that this group of A devices processed for this test had betas of ≈ 60 compared to ≈ 30 for the other A devices. The higher betas are thought to be due to their having shallower diffusion depths and correspondingly thinner protective layers than their lower beta counterparts. Based on the subsequently identified failure mechanisms, there is evidence in this case supporting a direct relationship between device beta and wearout rate.

VI. FAILURE ANALYSES

Accelerated stress testing is carried out to induce failures in a reasonable time in order to allow estimates of reliability. However, no reliability analysis is complete without the determination of the relationship between the device failure and its physical cause. Too often this analysis is very cursory and quickly terminated when some seemingly reasonable guess is made as to the probable cause of failure. To enhance diagnostic confidence levels, failure modes should be verified by duplicating the failures on special test structures simulating operating conditions.

Analysis of data indicates a degradation of the emitter-base junction ("leaky" emitter-base) related to stress levels in the MSC 1330. X-ray and scanning-electron-microscope analyses have been carried out at the Microwave Semiconductor Corporation and at the Naval Research Laboratory. A typical cell demonstrating the leaky emitter-base phenomenon is shown in Fig. 11. The dissolution of the SiO_2 and its reaction with Al to form Al_2O_3 + Si degrades the transistor junction passivators and eventually results in failure. Although the device could be made more resistant to this type of failure, device improvement may not be necessary for some applications if the same failure mode is still dominant at the lower stress levels. The sample calculations in Table IV using the extrapolated Arrhenius curve (Fig. 9) indicate device life in excess of 10^6 h for base-plate temperatures of 35°C. The thermal impedance is defined by measuring the peak junction temperature on the device during a pulse as a function of dissipated power. Therefore, for pulses which are short compared to the device thermal time constants, the thermal impedances are a function of pulsewidth. For Table IV, thermal impedances measured on life-tested 1330 devices were used. It is important to note that in actual operation the transistor peak junction temperature does not stay constant over the radar-system life. As the output power degrades, device dissipation is also reduced; hence the peak junction temperature decreases. For this reason, the reliability predictions shown in Table IV are conservative. The previously noted reliability calculations and Arrhenius extrapolations included in Table IV represent a more realistic system environment wherein the ambient or background temperature is assumed to be fixed at 35°C. Thermal impedances are functions of pulsewidth. In this case, the impedances measured during the MSC 1330 tests were used.

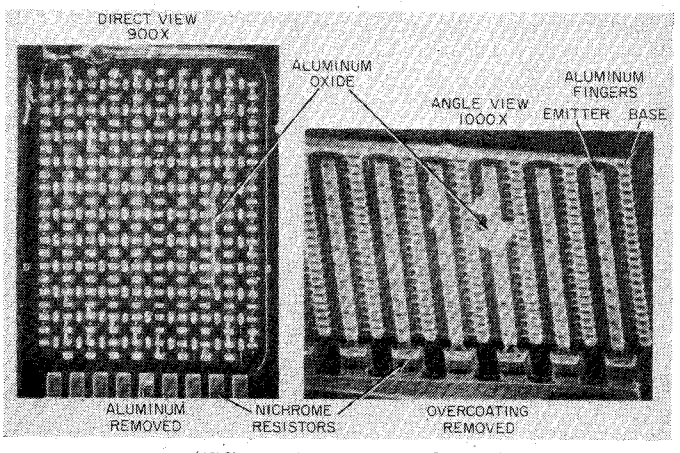


Fig. 11. MSC 1330 leaky emitter-base phenomenon.

These data clearly show the importance of device thermal impedance and collector efficiency in achieving long life. With this particular device geometry, the long life shown in Table IV cannot be expected at peak power levels much above 50 W unless the collector-efficiency thermal-impedance product is increased if the pulsewidth approaches the thermal time constants of the device.

Tests are in progress for the A device operating at 1.5-ms pulsewidth and 15-percent duty factor stressed at both 340°C and 280°C. These additional data are expected to further substantiate the present conclusions. However, it should be reemphasized that additional failure analysis and correlation with results from special test structures are necessary before it can be absolutely determined that the SiO_2 dissolution problem, in the case of the MSC 1330, is the direct cause of failure rather than the effect of some other wearout mechanisms not yet identified at these particular thermal stress levels. To aid in clarifying this problem, additional testing is also planned to determine the presence of any other dominant failure mechanism at lower stress levels. A 10 000-h test on the MSC 1330 operating at a peak junction temperature of 180°C is scheduled to begin in mid 1974.

VII. SUMMARY AND CONCLUSIONS

The stress test data for pulsed RF conditions presented indicate that solid-state devices appear promising for reliable solid-state radar. Sample calculations indicate how the systems designer can use accelerated test data. An example was given of failure modes which are not accelerated by high-temperature life tests.

Additional work now underway is required to evaluate devices from other manufacturers. Furthermore, efforts are required to accurately identify failure modes, propose fixes, and evaluate the effects of failure modes not accelerated by life tests. Longer term accelerated life tests at lower stress levels are now underway. These tests will reduce the potential errors from extrapolating over wide ranges of time, from life tests, to system use.

The present work indicates that reliable solid-state

radar arrays can be built in a 3–5-year time frame if well-defined, stringent processing controls are employed and adequate screening methods are evolved. However, reliable systems depend on a familiarity of the systems designer with factors affecting device reliability.

ACKNOWLEDGMENT

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REFERENCES

[1] D. J. Hoft and L. R. LaValle, "R.F. power modules for *L*-band solid state transmitters," presented at the IEEE S-MTT Int. Microwave Symp., 1974.
[2] A. Christou, W. Weisenberger, A. Macpherson, and H. Day, "Reliability studies on MSC, RCA, and PHI *L*-band power transistors," presented at the Government Microwave Application (GOMAC) Conf., 1974.
[3] W. Poole and L. Walshak, "Mean time to failure of an *L*-band power transistor under RF pulsed conditions," presented at the IEEE Reliability Physics Symp., Apr. 1974.

New Microwave-Frequency Synthesizers that Exhibit Broader Bandwidths and Increased Spectral Purity

PAUL G. TIPON

***Abstract*—A superior microwave-frequency synthesis technique is treated in this paper, emphasizing improved spectral purity with octave bandwidths in the microwave region. The microwave-frequency synthesizer is discussed in two sections each corresponding to a system unit. The driver unit specifications are analyzed in the first section, showing its voltage-controlled crystal oscillator (VCXO) $\mathcal{L}(f)$ output to be -130 dBc/Hz at 10 kHz. In the second section, the driver VCXO output is translated in the microwave unit to the final *X*-band frequency by means of a phase-locked loop. An analysis of this phase-locked loop, as described in this paper, shows the final $\mathcal{L}(f)$ equal to -101 dBc/Hz at 10 kHz. Since a worst case situation was assumed, the final $\mathcal{L}(f)$ is quite superior for octave bandwidth microwave-frequency synthesizers.**

NOMENCLATURE

f	Fourier frequency of fluctuations.
$\mathcal{L}(f)$	Normalized frequency domain measure of phase fluctuations; script $\mathcal{L}(f)$ is defined as the ratio of $\frac{\text{power density (one phase modulation sideband)}}{\text{power (total signal)}}$.
$S_{\delta\phi}(f)$	Spectral density of phase fluctuations.
δ	Fluctuation operator.
$\delta\phi$	Phase fluctuations.
ω	Fourier angular frequency of fluctuations $\omega \equiv 2\pi f$.
dBc	dB below the carrier.

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I. INTRODUCTION

A NEW microwave frequency synthesis technique has been introduced in a complete line of wide-band 0.5–18-GHz microwave sources with superior performance characteristics.[1] The microwave-frequency synthesizers using the new design exhibit a significant increase in spectral purity across an entire octave bandwidth. Thus the old limitations of tradeoff between bandwidth versus purity have been eliminated; and conveniences of remote programmability, resolution to 1 Hz, FM, AM, and PM capability, reparability, and low cost are still retained.

The technique discussed in this paper employs an indirect means of synthesis [1]. In this respect it is analogous to phase locking a microwave source to a VHF synthesizer. However, it also has a phase-locked crystal reference loop at microwave frequencies; and, in this manner, it is similar to a crystal-controlled microwave source. Both of these much used and well defined methods are employed in generating clean microwave signals. The new system consists of a synthesizer driver and a microwave-frequency synthesizer. The synthesizer driver uses indirect synthesis

[1] Patent pending.